REMARKS

Claims 1-34 are currently pending in the subject application, and are presently under consideration. Claims 1, 2, 5 - 7, 12, 13, 16, 21, 23, 24, 26 28 - 30, and 32 - 34 stand rejected. Claims 3, 4, 8 – 11, 14, 15, 17 – 20, 22, 25, 27, and 31 are objected to as being dependent from a rejected base claim, but would be allowable if rewritten in independent form. Claims 1, 7, 12, 21, 28, 30 and 33 have been amended. Favorable reconsideration of the application is requested in view of the amendments and comments herein.

I. Claim(s) 1, 28 - 30, and 32 - 34 are patentable over U.S. Patent No. 5,507,456.

Claim(s) 1, 28 - 30, and 32 - 34 stand rejected under 35 U.S.C. §102 as being anticipated by U.S. Patent No. 5,507,456 to Brown et al. ("Brown et al."). Withdrawal of this rejection is respectfully requested for at least the following reasons.

Brown et al. does not disclose an output waveform that temporarily adjusts to an intermediate level during a transition between normal high and low levels during a first operating mode, as recited in claim 1. Instead, Brown et al. teaches that a composite stepped-square waveform can be formed by selecting from different stepped square waves, such as shown in Figs. 2A, 2B, 2C and 2D. It is submitted that Brown et al contains no teaching that any combination of the waveforms would provide a control output that temporarily adjusts to an intermediate level during a transition between normal high and low levels, as recited in claim 1.

When the teaching of Brown et al. relative to Figs. 2A, 2B, 2C and 2D (e.g., see column 5 of Brown et al.) is properly considered in its entirety, however, it becomes evident that the amplitudes of the different waves 30, 31, 32 and 33 indicated at A1, A2, A3, A4 and A are disclosed as being different amplitudes. The waveform produced by the square wave generator of Brown et al. "are produced by a plurality of semiconductor switches connected with the transformer inputs which switches are selectably made to conduct so that the resulting waveform output obtains the desired stepped-square waveform." Brown et al. Col. 3, line 64, through Col. 4, line 1. Brown et al. continues to state that "the controller can selectively operate the semiconductor switches [via inputs 52, 54, 56, 58], thereby controlling the amplitude and duty cycle of the waveform which is produced by a particular transformer tap." Column 4, lines 4-7 of Brown et al. Moreover, when multiple waveforms are selected to provide the desired stepped

square waveform, the combined waveform has an additive effect which changes the high and low levels of the composite waveform accordingly. Since it is the selection of the transformer tap and the additive effect that determines the amplitude and duty cycle of the output stepped waveform (*e.g.*, by selecting a single or composite stepped waveform), Brown et al. does not disclose an output waveform that temporarily adjusts to an intermediate level during a transition between normal high and low levels during a first operating mode, as recited in claim 1. Any conclusion that Brown et al. discloses a waveform control according to claim 1 would be based on speculation not on what is taught in such reference.

The Office Action also states that "note that the intermediate level for the stepped-square wave is for a certain amount of time and thus Brown inherently includes a delay network that provides for this intermediate level." Applicants traverse this statement as an improper application of the doctrine of inherency. Specifically, an element of the claim is not inherent in the disclosure of the prior art unless extrinsic evidence clearly shows that the missing descriptive matter is necessarily present in the thing described in the reference, and inherency may not be established by mere probability or possibilities. See, e.g., *In re Robertson*, 49 U.S.P.Q.2d 1949 (Fed. Cir. 1999). There is nothing disclosed in Brown et al. that would require the circuitry of Brown et al. to include a delay network that controls the waveform control to provide the output at the intermediate level for a duration during the first operating mode, as recited in claim 1. The conclusion, based on inherency in the Office Action, thus appears based on speculation, which is insufficient to establish anticipation under 35 U.S.C. §102. For the reasons stated above, reconsideration and allowance of claim 1 is respectfully requested.

Claim 28 has been amended in a similar manner to claim 1. As a means plus function claim, claim 28 is construed under 35 U.S.C. §112, paragraph 6. Since, for substantially the same reasons stated above with respect to claim 1, Brown et al. does not teach means for controlling other recited means to temporarily modify a control signal to an intermediate level during a transition of the control signal between the normally high and low levels, claim 28 is not anticipated by Brown et al.

Claims 29 and 30, which are also written as a means plus function format, are allowable for at least the same reasons as claim 28. Additionally, claim 30 recites additional means for providing the output signal at an intermediate level that self-biases between the normal high and

low levels according to process variations in the system. The Office Action is silent as to any teaching in Brown et al. that might correspond to the means recited in claim 30. Applicants submit the failure to identify a teaching in Brown et al. is because Brown et al. is silent as to any structure capable of operating in a manner recited in claim 30. Since Brown fails to teach the system of claim 30, claim 30 should be allowed.

Claim 32, which depends from claim 28, further recites means for controlling a duration for which the control signal is provided at the intermediate level. Since Brown et al. fails to disclose means for controlling to modify the control signal temporarily to an intermediate level during a transition between the normally high and low levels (as recited in claim 28), Brown likewise does not teach that the switching controller (or other structure disclosed in Brown et al.) controls the duration that the control signal is provided at the intermediate level. It is submitted that any conclusion to the contrary is based on speculation and not on the express or inherent teachings of Brown et al. Reconsideration and allowance of claim 32 is respectfully requested.

Claim 33 has been amended to correct a typographical error and to recite that the delay is implemented to temporarily adjust the control signal to an intermediate level during a transition between normally high and low levels of the control signal. The method recited in claim 33 should be allowed for similar reasons as though stated above with respect to claim 28.

For the reasons described above, claim(s) 1, 28 - 30, and 32 - 34 should be patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

II. Claim(s) 1, 2, 5, 6, 12, 16, 21, 23, 24, 28, 29, 30, 30, 32, 33 and 34 are patentable over U.S. Patent No. 4,170,715.

Claim(s) 1, 2, 5, 6, 12, 16, 21, 23, 24, 28, 29, 30, 30, 32, 33 and 34 stand(s) rejected under 35 U.S.C. §102(b) as being clearly anticipated by U.S. Patent No. 4,170,715 to Mizokawa ("Mizokawa"). Withdrawal of this rejection is respectfully requested for at least the following reasons.

A complete reading of Mizokawa demonstrates divergent teachings in Mizokawa relative to the structure recited in the rejected claims. Specifically, at column 1, lines 13-19, Mizokawa specifically states that Mizokawa discloses a data communication system having two pulse signals having different pulse durations. This is in contrast to the recitation of amended claim 1 in which a waveform control provides a control output that temporarily adjusts a control output

to an intermediate level during a transition between high and low levels during a first operating mode and provides the control output to transition periodically between the high and the low levels during a second operating mode.

In support of the rejection of claim 1, the Office Action refers to Figs. 1-3 and corresponding portions of the description. Specifically, the Office Action states that the control output is provided at terminal "c" of Figs. 1 and 2, with further reference to transmission output C in Fig. 3. The Office Action contends that the control output at terminal "c" temporarily adjusts to an intermediate level between normal high and low levels during a first operating mode, namely when NRZ data is equal to one and SPM data is high. The Office Action then states that the second operating mode is defined by the case when the NRZ data is zero and the SPM data is don't care, either high or low. However, as depicted in Fig. 3 and as described in Mizokawa, nothing in Mizokawa teaches or suggests that the purported operating modes result in a temporary adjustment to the intermediate level during a transition between the normal high and low levels, as recited in claim 1. Instead, the relative output levels are determined as a function of the input signal provided at input "a" by controlling a transformer tap in element 24 of Mizokawa. The purported intermediate level of the transmission output "c" does not occur during a transition between normal high and low levels, as recited in amended claim 1.

The Office Action further states "[c]learly, the circuitry shown in Figures 1 and 2 inherently includes a delay network that sets forth i.e. controls the time of the intermediate level." Office Action, at page 3. The delay circuit implemented by "delay circuit 22 is selected that the delay times in the operation of the SPM circuit 1 and the amplitude level changing and transmitter circuit 30 (inverter 2 and drivers 3, 4 described later) may be compensated." That is, the delay circuit 22 synchronizes the NRZ transmission data signal at "a" with the split phase modulated signal at "b". The delay circuit 22 of Mizokawa does not control duration that the transmission output C is provided at an intermediate level, as the level of the transmission output C is solely a function of the input at "a" and the type of split phase modulation being implemented by SPM block 1. For similar reasons as stated with respect to Brown et al., Applicants submit that the circuitry in Figs. 1 and 2 does not include anything that expressly or inherently corresponds to the delay network recited in claim 1. The contention that Mizokawa discloses a delay network, as recited in claim 1, simply cannot be established by probabilities or

possibilities. Instead, extrinsic or intrinsic evidence must clearly show that the missing subject matter is necessarily present in order to anticipate. *In re Robertson*, supra. Since other circuitry than a delay network can be utilized and is disclosed as being utilized in Mizokawa, Mizokawa cannot anticipate claim 1.

Claim 2 further recites that the system of claim 1 also includes a driver that provides an output signal based on the control output provided by the waveform control. The output signal provided by the driver of claim 2 transitions between associated high and low levels during the second operating mode and transitions to an intermediate level for the duration during the first operating mode. The Office Action has failed to identify structure or teaching in Mizokawa corresponding to the driver recited in claim 2.

The Office Action states that elements 9 and 10 of the circuit in Fig. 2 of Mizokawa correspond to the driver recited in claim 2. With this reference, the Office Action states that the input to the driver is input "d" with the output of the circuitry 10 receiving input "d" being provided at output "e". As depicted in Fig. 4 of Mizokawa, however, the signal at output "e" of provided by the circuit 10 does not contain an intermediate level for the duration recited in claim 1; namely, the duration that is controlled by the delay network during the first operating mode. Instead, the reproduced output at "e" is provided at a "constant amplitude level." See column 2, lines 63-64 of Mizokawa. Since Mizokawa does not disclose a driver as recited in claim 2, Mizokawa does not anticipate claim 2. For these reasons, reconsideration and allowance of claim 2, as well as any rejected claims depending on claim 2, are respectfully requested.

Additionally, with respect to claim 5, the Office Action states that the signal at transmission output C, (as shown in Fig. 3) which is input to the driver at "d" (as the signal received input shown in Fig. 4), corresponds first and second control outputs provided by the waveform control to inputs of the driver, as recited in claim 5. However, as is evident from the description of Mizokawa, the signals depicted in Figs. 3 and 4, and the transmission output "c" and the input at "d", the transmission output "c" is only a single output that is provided via transmission line to input "d". To refer to transmission output "c" and the input at "d" as each containing multiple signals is a mischaracterization that is not only contrary what is disclosed in Mizokawa but also to well-known electrical engineering principles (*e.g.*, the current into the winding is equal to the current out of the winding). The relationship of single voltage signals

provided at "c" and "d" are evident by way of reference to Figs. 3 and 4 of Mizokawa. This is in contrast to the recitation in claim 5 in which a first control output is provided to a first input and a second control output is provided to a second input of the driver. Accordingly, reconsideration and allowance of claim 5 is respectfully requested.

The Office Action contends that "the waveform control 'self-biases' to the intermediate level..." This presumably is a reference to claim 6. However, claim 6 (depending from claims 5, 2 and 1) recites that the output signal self-biases to the intermediate level during the first operating mode based on relative characteristics of at least some devices that form the driver. Thus, in claim 6, it is the output signal, which is provided by the driver (recited in claim 2), that self-biases to its corresponding intermediate level. Additionally, the self-biasing of the output signal to the intermediate level occurs based on relative characteristics of components that form the driver, and not based on the waveform control as suggested in the Office Action. Since no structure is disclosed in Mizokawa to implement self-biasing as recited in claim 6, claim 6 is patentable. Reconsideration and allowance of claim 6 is respectfully requested.

With respect to claim 12, the Office Action further contends, without support of reference or teaching, the sources of the signals "a" and "b" constitute a predriver. Again, this contention appears to be based on speculation, and not based on proper inherency for a property or feature that must be present from the teachings of Mizokawa. See *In re Robertson*, supra. For example, signal b is split-phase modulated data provided by a split-phase modulation block "that has its voltage polarity inverted at every bit transition, as seen from FIG. 3." Mizokawa at Col. 3, lines 3-5. Additionally, there is nothing disclosed in Mizokawa and no intrinsic or extrinsic evidence to support the contention that a predriver is coupled to the control the system disclosed in Mizokawa to provide the signal at "a." Accordingly, claim 12 should be allowed.

Independent claim 16 recites a driver and a waveform controller. The waveform controller provides a control signal based on which the driver provides an output clock signal. As stated above with respect to claim 2, Mizokawa fails to teach (or even suggest) a driver that temporarily provides an output signal at an intermediate level between normally high and low levels during a second operating mode, as recited in claim 16. Instead, the circuit 10, which the Office Action identifies as the driver, provides its output at a constant amplitude level. See column 2, lines 63-64 of Mizokawa. Accordingly, Mizokawa does not anticipate claim 16.

Claim 21 has been amended to correct an inadvertent typographical error. The Office Action contends that element 24 in Fig. 2 of Mizokawa forms a divider that controls the amplitude during the second operating mode. However, no part of element 24 cooperates with any part of circuitry in the driver (namely circuit element 10 of Mizokawa), to form a voltage divider, as recited in claim 21. Thus, in addition to the structural deficiencies of Mizokawa, the functional interrelationship between portions of circuitry, as recited in claim 21, also are absent from the teachings of Mizokawa.

Claim 23 (depending from claim 16) recites that the output clock signal self-biases to the intermediate level during the second operating mode based on relative characteristics of at least some components that form the driver. The Office Action states that "the waveform control 'self-biases' to the intermediate level..." However, in claim 23 it is the output clock signal, which is provided by the driver, that self-biases. Additionally, the self-biasing to the intermediate level occurs based on relative characteristics of components that form the driver. Since no structure is disclosed in Mizokawa to implement the self-biasing as recited in claim 23, and certainly not components that form part of a driver (*e.g.*, elements 9 and 10) of Mizokawa, claim 23 is patentable. Reconsideration and allowance of claim 23 is respectfully requested.

With respect to claim 24, Applicants submit that no circuitry shown or disclosed in Mizokawa corresponds to a delay network that is capable of controlling a duration for which the output clock signal (provided by the driver of claim 16) is at the intermediate level during the second operating mode, as recited in claim 24. Instead, as stated above with respect to claim 2, the signal "e" is provided at a constant amplitude level, thus no circuitry in any controller or other circuit of Mizokawa controls the duration of the output clock signal as recited in claim 24. Reconsideration and allowance of claim 24 are respectfully requested.

Claim 28 has been amended to recite that the means for controlling controls the means for providing during a different operating mode to temporarily modify the control signal to an intermediate level during a transition of the control signal between the normally high and low levels. Claim 28 should be allowed for substantially similar reasons to those stated above with respect the waveform control of claim 1. Claims depending from claim 28 should also be allowed, and their allowance is respectfully requested.

Claim 30, which depends from claims 28 and 29, has been amended to correct a typographical error. Claim 30 recites means for providing the clock signal at an intermediate level that self-biases between normal high and low levels according to process variations in the system. The clock signal is provided by the means for providing introduced in claim 29, which provides the clock signal based on the control signal. As stated above with respect to claim 23, Mizokawa does not teach the self-biasing of a clock signal according to process variations in the system. Claim 30 thus should be allowable.

With respect to claim 32, the differences in the amplitude of the signal provided at "c" occur as a function of the input signal "a" through corresponding circuitry, and thus, does not control the duration at which a control signal is provided at an intermediate level according to the recitation of claim 32.

Claim 33 has been amended to recite that a delay is implemented to temporarily adjust the control signal to an intermediate level during a transition between the normally high and low levels during a second operating mode. Thus, for reasons similar those identified above with respect to claims 1 and 28, claim 33 should be allowed. Reconsideration and allowance of claim 33 is respectfully requested.

For the reasons described above, claim(s) 1, 2, 5, 6, 12, 16, 21, 23, 24, 28, 29, 30, 30, 32, 33 and 34 should be patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

III. Rejection of Claim(s) 13 and 26 Under 35 U.S.C. §103(a)

Claim(s) 13 and 26 stand(s) rejected under 35 U.S.C. §103(a) as being unpatentable over Mizokawa 4,170,715. Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claims 13 and 26 recite integrated circuits. The Office Action fails to identify in its rejection any teaching or suggestion in Mizokawa of an integrated circuit that might include the clock generator and circuit that is driven by the driver of the respective clock generator, as recited in claims 13 and 26. Instead, it is respectfully submitted that the system shown and disclosed in Mizokawa would not be implemented and integrated circuit as it includes

transformers and transmission paths corresponding to part of a broader communication system. Thus, claims 13 and 26 should be allowed.

For the reasons described above, claim(s) 13 and 26 should be patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

IV. Rejection of Claim(s) 7 Under 35 U.S.C. §103(a)

Claim(s) 7 stand(s) rejected under 35 U.S.C. §103(a) as being unpatentable over Mizokawa 4,170,715 in view of Nguyen et al., 6,781,416. Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claim 7 has been amended to correct an inadvertent typographical error noted by the Examiner. Additionally, it is respectfully submitted that the addition of Nguyen et al. fails to overcome the deficiencies noted above with respect to claims 6, 5 and 2 and 1 from which claim 7 depends. The Office Action contends that the push/pull driver shown and described with respect to Fig. 1 of Nguyen (*e.g.*, an inverter) could be substituted for the driver portion of Mizokawa. However, the use of the circuit in FIG. 1 of Nguyen as a substitution for driver circuitry in Mizokawa, as suggested in the Office Action, fails to meet the recitation of claim 7. Specifically, claim 7 states that transistor of a first type is associated with a first input of a driver and transistor of a second type is associated with a second input of a driver. In contrast, the push/pull driver of Nguyen has a single input, indicated at 3 in Fig. 1. Accordingly, the proposition to combine Nguyen with Mizokawa, as suggested in the Office Action, appears to contradict the earlier contention with respect to claim 5 in which the Office Action states that signals at "c" and "d" each have multiple inputs, where "d" is the input to the driver. Furthermore, there is no suggestion or teaching in either Nguyen or Mizokawa that would provide proper motivation to enable the relative strength of the respective first and second types of transistors be utilized to provide for the self-biasing to the intermediate level as recited in claim 7.

For the reasons described above, claim(s) 7 should be patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

V. Allowable Subject Matter

Applicants appreciate the indication of allowable subject matter with respect to claims 3, 4, 8-11, 14, 15, 17, 18-20, 22, 25, 27 and 31.

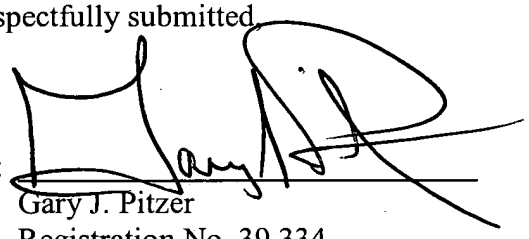
VI. CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Should the Examiner have any questions regarding this response or believe that a telephone interview would be helpful to prosecution of the subject application, the Examiner is invited and encouraged to contact Applicant's undersigned attorney at (216) 621-2234, Ext. 106.

In the event any additional fees or credits are due in connection with the filing of this document, the Commissioner is also authorized to charge fees or credit overpayments to Deposit Account No. 08-2025.

Respectfully submitted,

By: 

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